IN THE CLAIMS

Please cancel Claims 1 and 8 without prejudice or disclaimer.

Claim 1 (cancelled).

Claim 2 (previously presented): A method according to claim 4 wherein the sampling step further comprises converting of an analog actuator voltage into a digital actuator voltage sample signal.

Claim 3 (previously presented): A method according to claim 4 wherein the step of applying the digital voltage command to control the actuator voltage further comprises converting the digital voltage command into an analog voltage level.

Claim 4 (previously presented): In a hard drive assembly having an actuator, the actuator having an actuator voltage, a method of controlling the actuator comprising the steps of:

sampling the actuator voltage;

processing an actuator voltage sample for generating a digital voltage command;

applying the digital voltage command to control the actuator voltage,

wherein the step of applying the digital voltage command to control the actuator voltage further comprises using pulse width modulation.

Claim 5 (previously presented): A method according to claim 4 wherein the step of sampling the actuator voltage further comprises steps of:

putting the actuator in a high impedance state;

waiting for an actuator current to reach approximately zero; and

thereafter sampling the actuator voltage.

PAGE 4/10 * RCVD AT 2/20/2006 3:48:27 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/25 * DNIS:2738300 * CSID:972 917 4417 * DURATION (mm-ss):02-38

Claim 6 (previously presented): A method according to claim 4 wherein the step of processing the digital actuator voltage sample for generating a digital voltage command further comprises steps of calculating a velocity error and applying velocity error compensation to the digital voltage command.

Claim 7 (previously presented): In a hard drive assembly having an actuator, the actuator having an actuator voltage, a method of controlling the actuator according to claim 4 further comprising steps of, subsequent to the applying step, waiting for a selected time interval and reiterating the sampling, processing, and applying steps.

Claim 8 (cancelled).

Claim 9 (previously presented): A method according to claim 11 wherein the step of calculating a BEMF may be described by the formula,

BEMF = Vmtr – Imtr * Rmtr [Equation 2], wherein

Vmtr represents actuator motor voltage,

Imtr represents actuator current, and

Rmtr represents actuator motor resistance.

Claim 10 (previously presented): A method according to claim 11 wherein the step of calculating a velocity error, Ev, may be described by the formula,

Ev = Vtgt – BEMF [Equation 3], wherein

Vtgt represents target actuator voltage, and

BEMF represents the actual voltage across the actuator.

Claim 11 (previously presented): In a hard drive assembly having an actuator, the actuator having an actuator voltage, a method of controlling the actuator comprising the steps of:

sampling the actuator voltage;

sampling an actuator current;

PAGE 5/10 * RCVD AT 2/20/2006 3:48:27 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/25 * DNIS:2738300 * CSID:972 917 4417 * DURATION (mm-ss):02-38

calculating a BEMF using the sampled actuator voltage and sampled actuator current;

calculating a velocity error using the BEMF and a selected target voltage;

producing a digital voltage command for compensating the actuator voltage for the velocity error; and

applying a voltage at the actuator according to the digital voltage command,

wherein the digital voltage command, Vcmd, may be described by the formula,

Vcmd = ki * [x(n) + x(n-1)] + yi(n-1) + kp * x(n) + ffwd [Equation 4],

wherein,

ki is a constant representing the magnitude of integral compensation to apply,

x(n) is a sample of the current value of the error term Ev,

yi represents the output of the integral portion of the compensation, and

ffwd represents a feed forward voltage that allows the loop to run with a zero error within the dynamic range of the integrator.

Claim 12 (previously presented): In a hard drive assembly having an actuator, the actuator having an actuator voltage, a method of controlling the actuator according to claim 11 further comprising the steps of, subsequent to the applying step, waiting for a selected time interval and reiterating the foregoing steps.

Claim 13 (original): A velocity-controlled actuator apparatus in a hard drive assembly having an actuator motor, the velocity-controlled actuator apparatus comprising:

a sampler for sampling an actuator motor voltage and outputting a digital actuator motor voltage sample;

a timer for periodically activating the sampler; and

a digital processing engine for receiving a target actuator voltage command and the digital actuator motor voltage sample and for outputting a digital voltage command for controlling the actuator motor.

PAGE 6/10 * RCVD AT 2/20/2008 3:48:27 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/25 * DNIS:2738300 * CSID:972 917 4417 * DURATION (mm-ss):02-38

Claim 14 (original): A velocity-controlled actuator apparatus according to claim 13 wherein the timer is further adapted for putting the actuator motor in a high impedance state.

Claim 15 (original): A velocity-controlled actuator apparatus according to claim 13 further comprising a digital-to-analog converter for receiving the digital processing engine digital voltage command and outputting an analog voltage.

Claim 16 (original): A velocity-controlled actuator apparatus according to claim 13 further comprising an analog-to-digital converter operatively coupled to the actuator motor and sampler for sampling an analog actuator voltage and providing a digital signal to the sampler.

Claim 17 (original): A velocity-controlled actuator apparatus according to claim 13 wherein the digital processing engine further comprises a gain component for providing a pre-selected output gain.

Claim 18 (original): A velocity-controlled actuator apparatus according to claim 13 wherein the digital processing engine further comprises an integrator for calculating the digital voltage command.

Claim 19 (original): A velocity-controlled actuator apparatus according to claim 13 wherein the digital processing engine further comprises a digital processing engine shared by other functions in the hard drive assembly.

Claim 20 (original): A velocity-controlled actuator apparatus according to claim 13 wherein the digital processing engine further comprises machine readable instructions according to Table 1.

PAGE 7/10 * RCVD AT 2/20/2006 3:48:27 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/25 * DNIS:2738300 * CSID:972 917 4417 * DURATION (mm-ss):02-38

Claim 21 (original): A velocity-controlled actuator apparatus according to claim 13 wherein the digital processing engine further comprises machine readable instructions according to Table 2.

Claim 22 (original): A velocity-controlled actuator apparatus according to claim 13 wherein the digital processing engine further comprises machine readable instructions according to Table 3.

PAGE 8/10 * RCVD AT 2/20/2006 3:48:27 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/25 * DNIS:2738300 * CSID:972 917 4417 * DURATION (mm-ss):02-38